IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Amended) A feed forward circuit for reducing delay through an input buffer, comprising:

an inverter having an input and an output, the inverter being defined by transistors of a first size and powered by a first voltage level;

an inverting circuit having an input and an output, the input of the inverting circuit being coupled to the output of the inverter, the inverting circuit being defined by transistors of the first size and powered by a second voltage level that is lower than the first voltage level, the inverting circuit being powered by the second voltage level enables transitioning to the second voltage level; and

a feed forward transistor of a second size that is smaller than the first size has ~~having~~ a gate coupled to the input of the inverter and powered by the second voltage level, and the feed forward transistor further having a terminal coupled to the output of the inverting circuit, wherein the feed forward transistor decreases an amount of time required for the output of the inverting circuit to change state when the inverting circuit is powered by the second voltage level.

2. (Original) A feed forward circuit as recited in claim 1, wherein the decrease in the amount of time required for the output of the inverting circuit to change state is at least one gate delay of the inverting circuit.

3. (Original) A feed forward circuit as recited in claim 1, wherein the feed forward transistor increases a voltage at the output of the inverting circuit when the input to the inverter transitions to a HIGH state.

4. (Original) A feed forward circuit as recited in claim 1, wherein the feed forward transistor ceases to increase the voltage at the output of the inverting circuit when the input to the inverter transitions to a LOW state.

5. (currently amended) A feed forward circuit as recited in claim 1, wherein the inverting circuit includes a p-channel transistor and an n-channel transistor, the p-channel transistor having a first terminal coupled to the second voltage ~~a core voltage~~, a gate coupled to the input of the inverting circuit, and a second terminal coupled to a first terminal of the n-channel transistor, the n-channel transistor having a gate coupled to the input of the inverting circuit.

6. (Original) A feed forward circuit as recited in claim 5, further comprising a high impedance transistor coupled to a second terminal of the n-channel transistor of the inverting circuit, the high impedance transistor having a terminal coupled to ground.

7. (Original) A feed forward circuit as recited in claim 6, further comprising a low impedance transistor coupled to the second terminal of the n-channel transistor of the inverting circuit, the low impedance transistor having a terminal coupled to ground, wherein the low impedance transistor is ON when the output of the inverting circuit is HIGH.

8. (Original) A feed forward circuit as recited in claim 7, wherein the low impedance transistor is OFF when the output of the inverting circuit is LOW.

9. (Original) A feed forward circuit as recited in claim 1, wherein the feed forward transistor turns off, allowing the voltage at the output of the inverting circuit to transition to a LOW state when the input to the inverter transitions to a LOW state.

10. (Original) A feed forward circuit as recited in claim 1, wherein the inverting circuit includes an n-channel transistor and a p-channel transistor, the n-channel transistor having a first terminal coupled to ground, a gate coupled to the input of the inverting circuit, and a second terminal coupled to a first terminal of the p-channel transistor, the p-channel transistor having a gate coupled to the input of the inverting circuit.

11.- 25. (Cancelled)

26. (New) A feed forward circuit for reducing delay through an input buffer as recited in claim 1, wherein the first voltage level is ring voltage.

27. (New) A feed forward circuit for reducing delay through an input buffer as recited in claim 1, wherein the second voltage level is core voltage.

28. (New) A feed forward circuit for reducing delay through an input buffer as recited in claim 1, wherein the first size transistors are I/O ring size transistors and the second size transistors are core size transistors, and the first size transistors are larger than the second size transistors.